**Specification Amendments**

Please replace paragraph 0016 with the following rewritten paragraph:

0016 Referring to Figure 1B, in an important aspect of the present invention, following removal of the resist layer 16, for example by an oxygen ashing and/or a wet stripping process, a conventional silicon dry (plasma assisted) etch process is carried out to etch through a thickness portion of the silicon substrate 12 to form a recessed opening area e.g., 12B using the silicon oxide opening e.g., 14B as an etching mask. It will be appreciated that the depth of the recessed opening area 12B is adjustable depending of on MOSFET design rules, and depending on the depth of a subsequently formed S/D extension (SDE) implant depth. For example, preferably, the recessed opening 12B is formed at a depth with respect to the adjacent upper portion of the silicon substrate 12, of about 200 Angstroms to about 500 Angstroms. For example, the total depth of adjacent source/drain extension (SDE) doped regions as shown below are preferably formed to be less than about 1600 Angstroms. Preferably, the lower portion of the subsequently formed SDE regions is about a factor of about 3 times to about 6 times the depth of the recessed area 12B.

Please replace paragraph 0025 with the following rewritten paragraph:

0025 Following the S/D doping process, optionally salicide portions e.g., 30A, 30B, and 30C, for example $TiSi_2$ or Co[[O]]$Si_2$, are formed over the S/D regions and polysilicon electrode portion by conventional processes to complete formation of the MOSFET device.

Please replace paragraph 0027 with the following rewritten paragraph:

0027 For example, subsequent elevated temperature processing steps causes increased vertical as well as lateral diffusion of the SDE region dopants [[r]], thereby degrading device performance, including increased short channel effects such as current leakage ($I_{off}$ leakage) while reducing $I_{drive}$. In addition, the reduced width of the gate oxide portion, e.g., 12C, reduces overlap capacitance including drain to gate overlap capacitance thereby improving both high frequency analog and digital device operation. The overlap capacitance is also advantageously reduced by reducing lateral dopant diffusion according to the structure and method of the present invention, for example, by reducing lateral dopant diffusion from the SDE regions 25A, 25B to the doped channel region e.g., 32.